MOSFET Channel Engineering and Scaling Study using COMSOL® Multiphysics Simulation Software

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Abstract — With the scaling of semiconductor devices into the nanometer regime, short channel effects such as threshold voltage instability, reduced output resistance, punchthrough and hot-electron degradation persist. COMSOL Multiphysics is used to study the effect of constant-field scaling on a FIBMOS device compared to the conventional MOSFET. A MOSFET is made using doping models. A narrow P+ region is implanted next to the source region to emulate a FIBMOS device. Building on the previous work done by Shen et al., we conduct simulations on conventional MOSFETs as well as FIBMOS transistors for 122.5-nm, 175-nm, 245-nm, and 350-nm channel-length devices. The simulations show that the FIBMOS device demonstrates greater threshold voltage stability upon channel length variation, improved output resistance, greater resistance to the punchthrough effect, and reduced hot electron degradation.

Keywords: FIBMOS, MOSFET, Constant Field Scaling, COMSOL Multiphysics

1 Introduction

In past decades, MOSFETs have been engineered to be smaller, faster and more efficient. As the device gets smaller, the circuit delay time and power dissipation per device get smaller. Hence, the device gets faster and more efficient [1]. This continuous reduction of the transistor size over the decades has helped industry to make our smartphones, computers and other devices drastically faster, more reliable, more power efficient, and cheaper. As the demand for speed, reliability, and efficiency increases, the transistors are bound to be designed smaller. However, as the transistors get very small, the short channel effects come into play. While designing transistors in the nanoscale regime, researchers have to think about diminishing the short channel effects and hot-carrier degradation. Minimizing the short channel effects such as drain-induced barrier lowering, punch-through effect, and threshold voltage instability requires implementation of high substrate doping density. Improving hot-carrier reliability such as decreasing impact ionization, substrate current, and hot electron injection requires lower electrical field, and therefore, lower substrate doping density.

Numerous efforts have been made by the researchers and scientific community to optimize the semiconductor device in order to achieve the optimal balance between conflicting requirements. This effort has yielded different device structures such as halo implant, Lightly Doped Drain (LDD), and FIBMOS. FIBMOS is proposed for channel engineering in high-performance MOSFETs. Shen and his co-workers have shown, using a 350-nm device, that FIBMOS exhibits higher output resistance, reduced hot electron degradation, and reduced punch-through effect [2]. This paper builds on the work done by Shen et al. We use COMSOL Multiphysics to compare the effects of Constant Field Scaling on a FIBMOS device compared to those on a conventional MOSFET. We try to examine the different characteristics exhibited by the FIBMOS and also analyze if use of FIBMOS can avoid the short channel effects and hot-carrier degradation when scaled down.

The asymmetric doping profile in the FIBMOS device prevents us from using the classical expressions for the calculation of current, threshold voltage, and electrical field inside the device as they are rather a complex function of doping density and step doping width [3]. The traditionally used formulae are approximations that work well for larger devices, but are unacceptable for small devices. Simulation of these devices requires numerically solving the fundamental semiconductor equations at numerous points in the device. COMSOL provides multiple modules and sets of equations which can be applied to solve for a given condition. This builds up the required infrastructure to design specific devices and conduct required simulations.

2 Device Structure

The general structure of a FIBMOS device is similar to a MOSFET but with a narrow P+ region next to the source region. Figure 1 shows the schematic diagram of the FIBMOS device that is being simulated in this research.

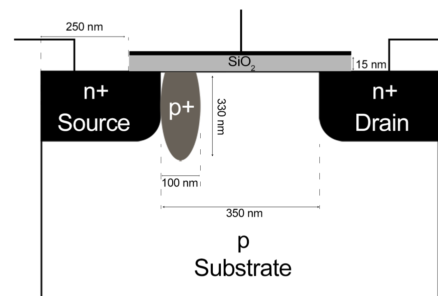

Figure 1. Schematic description of the structure and doping profile of the FIBMOS device with gate length of 350 nm and oxide thickness of 15 nm.

Using COMSOL Multiphysics with the Semiconductor Module (semi), the 2D models of the devices are designed. The transistors are constructed using silicon, and regions with different doping concentrations have been implemented. A narrow P+ region with higher doping concentration than the substrate is implanted next to the source region to emulate an asymmetric device structure that is made using the Focused-Ion-Beam technique. A Gaussian doping profile is used for both source/drain junction and p-p+ junction. The drawn channel length of both conventional MOSFET and FIBMOS devices is 350-nm. The source and drain extension is 250-nm. The substrate doping for both devices is the same. For the FIBMOS device, the length of the P+ region is 100-nm and the depth is 330-nm. The doping density and other dimensions of the 350-nm devices are listed in Table 1.

Table 1. Dimensions and doping densities of the devices

Parameter	Conventional	FIBMOS
Substrate doping	5×10^{16} cm^{-3}	5×10^{16} cm^{-3}
Source Drain doping peak	7×10^{20} cm^{-3}	7×10^{20} cm^{-3}
P+ Region doping peak	1×10^{19} cm^{-3}	—
Oxide Thickness	15 nm	15 nm
Gate Width	20 μm	20 μm
Junction depth	130 nm	130 nm

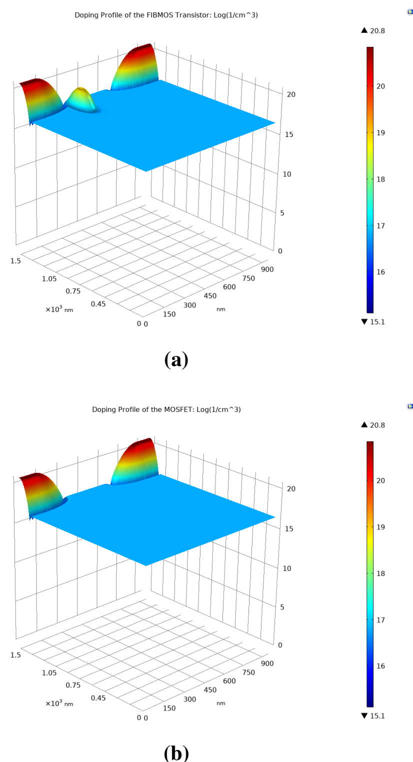

Figure 2. Doping Profile of (a) FIBMOS device and (b) Conventional MOSFET

3 Method

3.1 Theory

Fabrication of short-channel transistors requires use of degenerate doping. For a non-degenerate semiconductor, the doping density is low and the donor electrons do not interact. Hence, we can use the Maxwell-Boltzmann approximation to calculate the electron concentration. As the doping density is increased, the electrons start to interact. When the concentration of electrons in the conduction band exceeds the density of states N_c, the Fermi level lies within the conduction band rendering the Maxwell-Boltzmann approximation invalid. Therefore, Fermi-Dirac statistics have been used for determining carrier concentrations. The Fermi function provides the probability that an energy level at energy E, in thermal equilibrium with a large system, is occupied by an electron. The system is characterized by its temperature, T, and its Fermi energy, E_F [4]. The Fermi function is given by:

$$f(E) = \frac{1}{1 + exp(\frac{E - E_F}{kT})} \tag{1}$$

Multiple factors affect the mobility of the carriers inside the semiconductor which makes it a complex function of temperature, electrical field, and doping density. Different models have been developed in order to encapsulate those effects for simulation purposes [5]. The effects on mobility of the carriers due to phonon scattering, ionized impurity scattering, carrier-carrier scattering, interface charges, and presence of large electric fields have been addressed by incorporating Mobility Models into the simulator. Recombination of the carriers due to imperfections in the device has been considered by implementing the Shockley-Read-Hall Recombination Model. The solver setting for the simulator is changed in order to facilitate the employed mobility models and achieve convergence.

The simplistic nature of the drift-diffusion equations makes them appealing to use for the simulations. However, when the semiconductors are scaled down to the sub-micrometer regime, the assumptions made for the drift-diffusion model lose their validity. In order to simulate small devices, in which the interaction of electrical and thermal phenomena play an important role, the assumption of an isothermal temperature profile is invalid. Hence, the heat-conservation equation has to be solved along with the semiconductor equations [6]. The full hydrodynamic method is complicated due to its hyperbolic nature. So, the energy-transport (or energy balance model) is used in the simulation [7]. This accounts for heat-conservation. In addition to drift and diffusion currents, there is an additional current due to thermal gradients in the carrier temperature [6]. This modifies the carrier transport equations which take the form of Equation (4).

3.2 Mesh

Two different user-controlled meshes are generated according to the needs of the simulations. The mesh in figure 3(a) consists of 24592 domain elements and 398 boundary elements and was the mesh primarily used. The mesh in figure 3(b) consists of 25910 domain elements and 1068 boundary elements and is used to extract the electrical field and electron concentration at the surface.

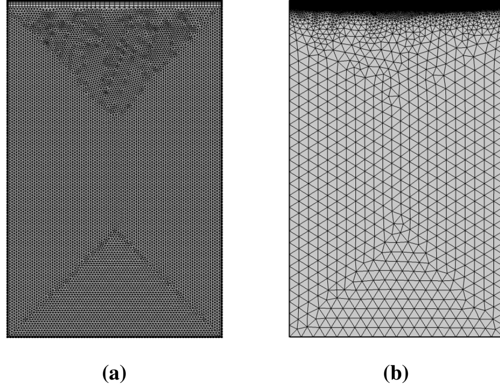

Figure 3. Two meshes used for the simulation

3.3 Equations used

Simulating a semiconductor device requires solving the Poisson and continuity equations. The Semiconductor Module provided the complete set of equations and their dependencies. The Poisson equation, derived from Maxwell's Equations, is used in tensor form:

$$\nabla \cdot (-\varepsilon_0 \varepsilon_r \nabla V) = q(p - n + N_d^+ - N_a^-) \qquad (2)$$

where q is the elementary electron charge, p is hole concentration, n is electron concentration, and N_d^+ and N_a^- are charged impurities of donors and acceptors, respectively. Continuity equations, also derived from Maxwell's Equations, are given by:

$$\begin{aligned} \frac{\delta n}{\delta t} &= \frac{1}{q}(\nabla \cdot J_n) - U_n \\ \frac{\delta p}{\delta t} &= -\frac{1}{q}(\nabla \cdot J_p) - U_p \end{aligned} \qquad (3)$$

where J_n and J_p are electron and hole current density, respectively, $U_n = \Sigma R_{n,i} - \Sigma G_{n,i}$ is the net electron recombination rate from all generation $(G_{n,i})$ and recombination $(R_{n,i})$ mechanisms , and U_p is the net hole recombination. J_n and J_p are given by the following equations:

$$\begin{aligned} J_n &= qn\mu_n \nabla E_c + \mu_n k_B T G(\frac{n}{N_c}) \nabla n + qnD_{n,th} \nabla ln(T) \\ J_p &= qp\mu_p \nabla E_v + \mu_p k_B T G(\frac{p}{N_v}) \nabla p + qpD_{p,th} \nabla ln(T) \end{aligned} \qquad (4)$$

where μ_p and μ_n are hole and electron mobility, respectively, k_B is the Boltzmann constant, $D_{p,th}$ and $D_{n,th}$ are hole and electron thermal diffusion coefficients, respectively, N_c and N_v are the effective densities of states for the conduction and valence bands, respectively, and T is temperature. The function $G()$ is defined as:

$$G(\alpha) = \frac{\alpha}{F_{-\frac{1}{2}}(F_{\frac{1}{2}}^{-1}(\alpha))} \qquad (5)$$

where $F_r()$ is the complete Fermi-Dirac integral of order r.

In order to achieve higher fidelity, mobility models were implemented in a stack form i.e. one on top of another.

$$\mu_{total} = \mu_E(\mu_S(\mu_C(\mu_{LI})))$$

where μ_E, μ_S, and μ_C are functions that address the effects of mobility due to high field velocity scattering, surface scattering, and carrier-carrier scattering, respectively. μ_{LI} is the mobility model for phonon and impurity scattering.

3.4 Constant-Field Scaling

The constant field scaling approach is used to scale down the device. The parameters of the devices are scaled by the factors described in Table 2.

Table 2. Constant field scaling

Parameter	Scaling factor ($k < 1$)
Channel length	k
Source/Drain extension	k
Junction Depth	k
Gate Oxide Thickness	k
Doping Density	$1/k$
FIB implant width	1

The size of a MOS transistor is generally reduced by a factor of 0.7 in each technology generation to halve the area of the transistor. We scale down the device using a parametric sweep on k (scaling parameter) for values of 1, 0.7, 0.5, and 0.35 that would yield devices with drawn channel lengths of 350-nm, 245-nm, 175-nm, and 122.5-nm, respectively. We measure the quantities such as drain current, electrical field, and electric potential as we run the simulation with varying drain-source voltage, gate-source voltage, and size of the devices.

4 Results and Discussions

4.1 Threshold stability

A simulation study is conducted for different values of gate voltage. Drain current is analyzed to get the Transfer Characteristics of the device. The drain-source voltage is 10mV for the 350-nm device and is scaled by the factor of k as the device is scaled down. As shown in figure 4, the

FIBMOS device shows threshold stability over the channel lengths while the threshold voltage of the conventional MOSFET decreases as the device is scaled down. Since, the threshold voltage for FIBMOS is a function of the width and dose of the FIB implant [3], it remains almost constant.

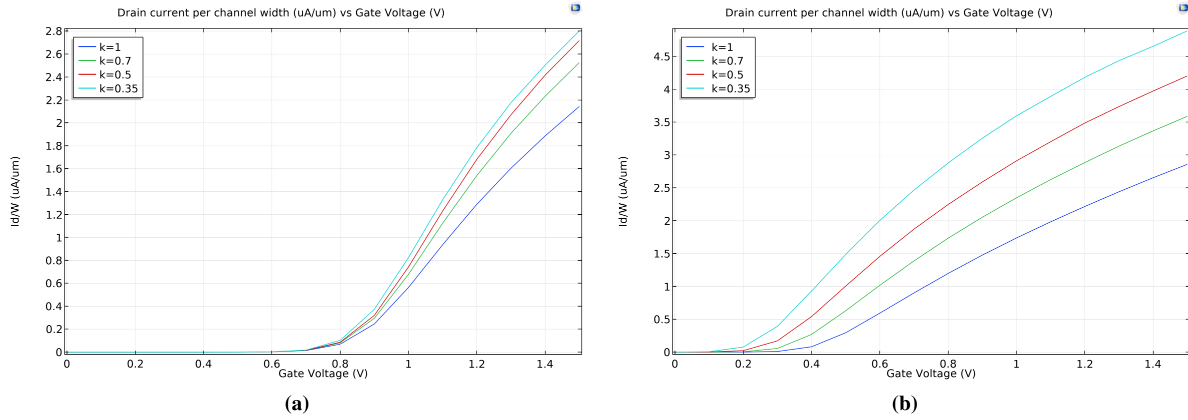

Figure 4. Transfer Characteristics of (a) FIBMOS device and (b) Conventional MOSFET

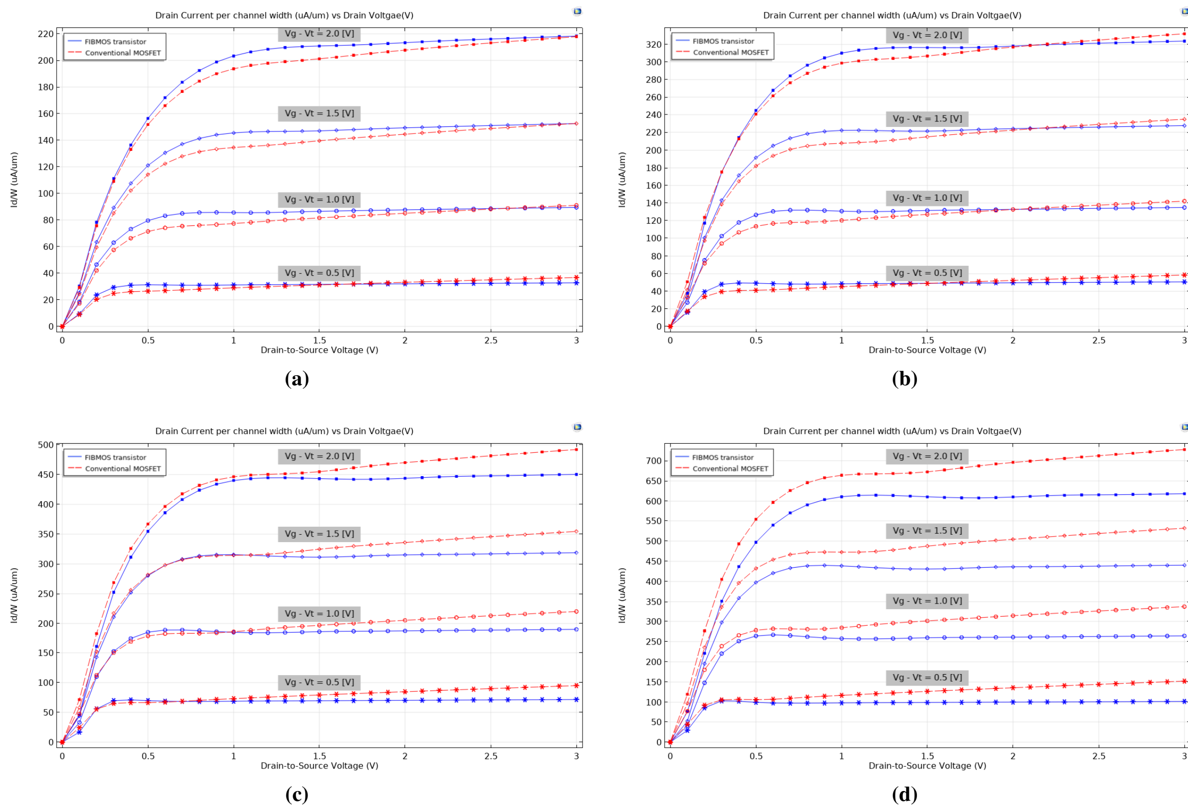

Figure 5. Output Characteristics of FIBMOS device and conventional MOSFET for channel length of (a) 350-nm, (b) 245-nm, (c) 175-nm, and (d) 122.5-nm

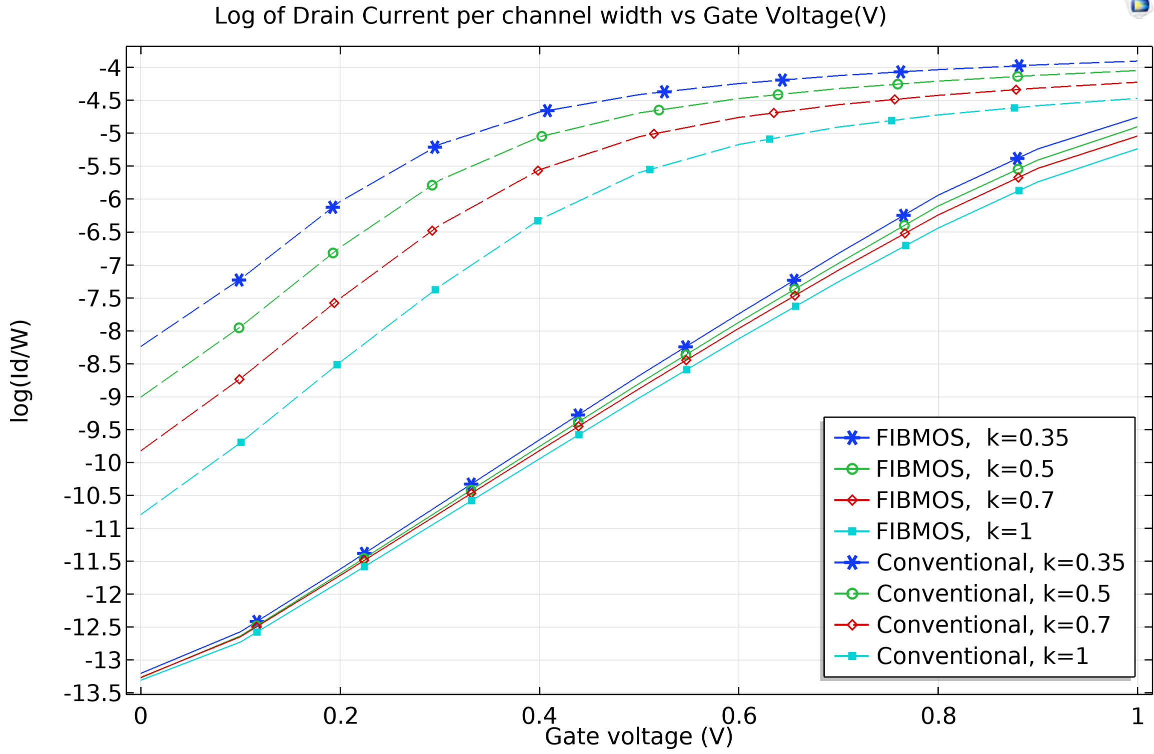

Figure 6. Subthreshold conduction of the FIBMOS device and conventional MOSFET

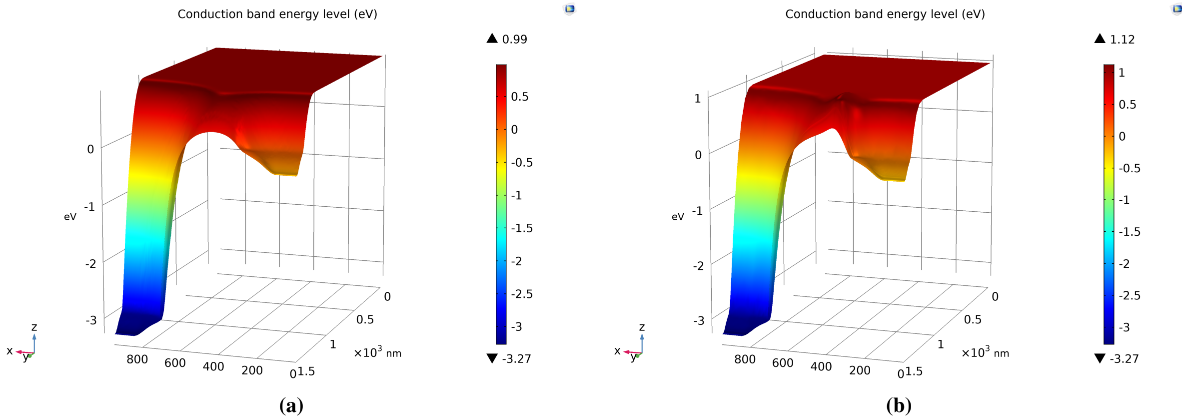

Figure 7. Conduction band energy level of (a) Conventional MOSFET and (b) FIBMOS device with applied biases: $V_g = 0V$ and $V_{ds} = 3V$

4.2 Improved Output Resistance

Figure 5 shows the comparison of the output characteristics between the conventional MOSFET and the FIBMOS devices. In the saturation region, the FIBMOS device has almost zero slope while the conventional MOSFET shows a significant amount of slope. This proves that the FIBMOS device has higher output resistance. A similar trend is shown in work done by Shen et. al [2]. This increase in output resistance can be explained by the total carrier concentration. Figure 8 shows the electron concentration at the surface near the gate. The electron concentration for FIBMOS is higher near the drain region. This leads to the pinchoff region for FIBMOS being shorter. The output resistance is negatively correlated to the ratio of pinchoff

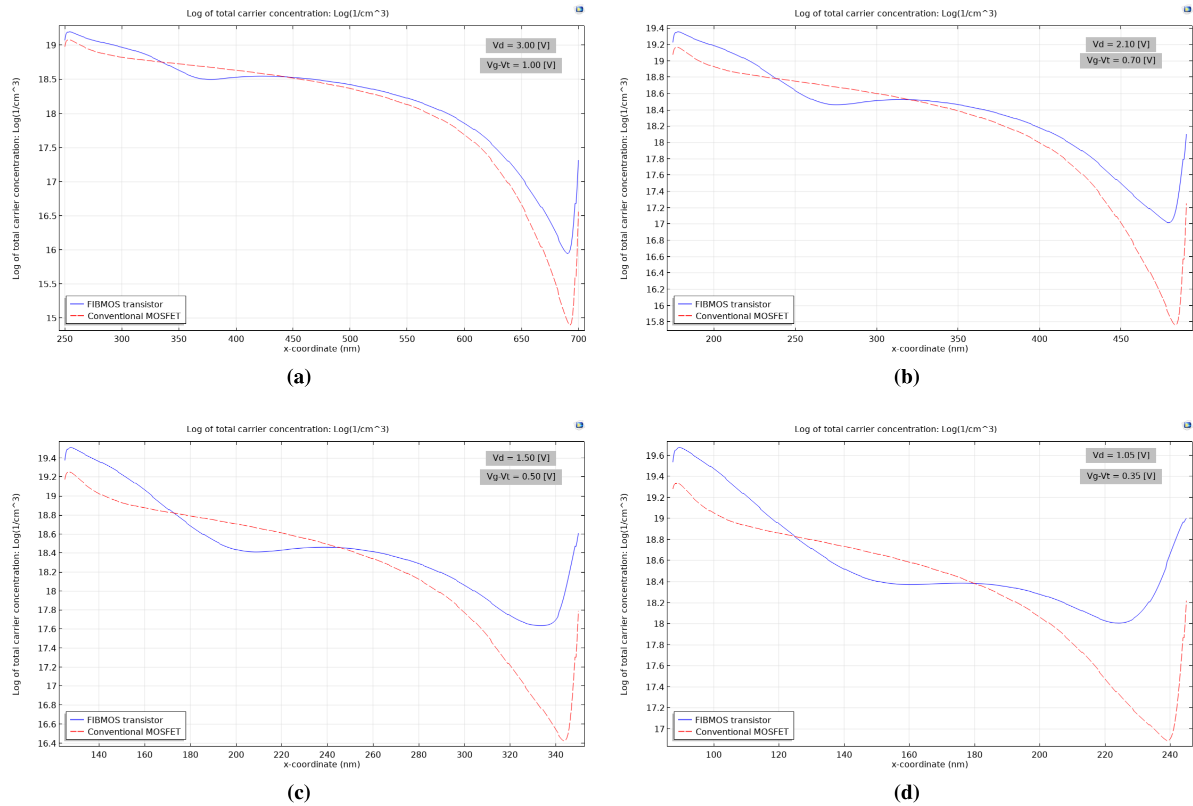

Figure 8. Electron concentration at surface near gate of FIBMOS device and conventional MOSFET for channel length of (a) 350-nm, (b) 245-nm, (c) 175-nm, and (d) 122.5-nm

length and channel length. Therefore, a shorter pinchoff region results in greater output resistance.

4.3 Greater Resistance to punchthrough effect

The ideal current-voltage relationship assumes zero drain current when the gate-source voltage is less than the threshold voltage. Experimentally, there is a small non-zero drain current [1]. This problem is magnified in short-channel devices because of DIBL. This leads to current leakage and power consumption in stand-by mode. A simulation study is done in the subthreshold region of the transistors. The drain-source voltage for the 350-nm channel device is 0.5 V and is scaled by a factor of k as the device is scaled. In figure 6, we can see the subthreshold current in the FIBMOS device is very low and is consistent as the device is scaled down. The subthreshold current for the conventional MOSFET increases as the device is scaled down. The improvement in punchthrough resistance in FIBMOS can be attributed to the FIB implant. As seen in figure 7, a higher doping density region creates a potential barrier which prevents the depletion region from spreading from drain to source.

4.4 Higher resistance to hot electron degradation

A simulation study is done to analyze the lateral electrical field at the surface near the interface. For 350-nm devices biases are: $V_{ds} = 3.0V$ and $V_g - V_t = 1.0V$. As the device is scaled down, the drain-source voltage and the difference between the gate and threshold voltage is scaled by a factor of k. Figure 9 shows the lateral electrical field for the FIBMOS device and the conventional MOSFET. It is clear that the lateral drain electrical field is consistently higher for the conventional MOSFET. Hot electron degradation is exponentially dependent on the magnitude of the lateral drain electrical field [2]. Therefore, FIBMOS devices show significant improvement against hot electron degradation.

5 Conclusion

In industry, fabrication and design of semiconductor devices requires simulation results in order to predict device performance. This reduces expenditure in time and money. COMSOL provides numerous modules that are useful in predicting and visualizing current, electrical field, and carrier concentrations of a device. Implementation of

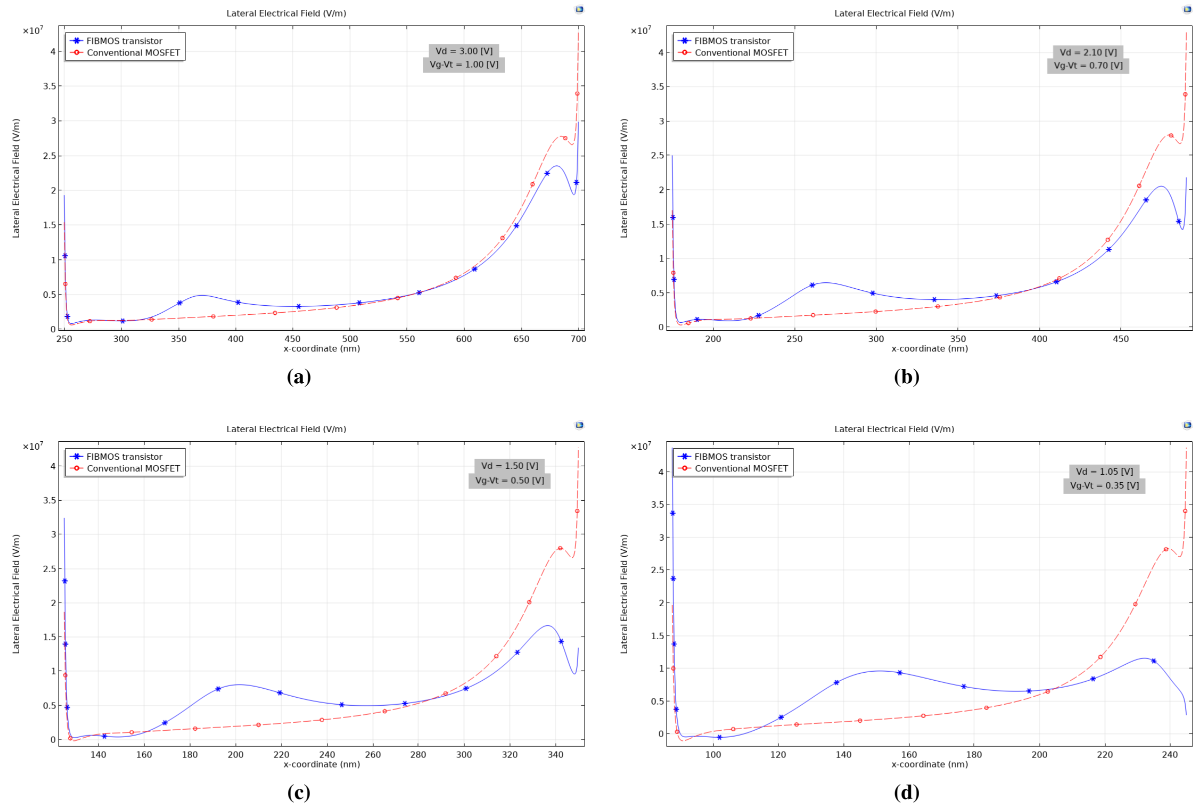

Figure 9. Lateral Electrical Field at surface near gate of FIBMOS device and conventional MOSFET for channel length of (a) 350-nm, (b) 245-nm, (c) 175-nm, and (d) 122.5-nm

various simulation models makes it able to predict results with high fidelity. The result produced agrees with previous work done by Shen et al. [2], and the trend continues for shorter channel lengths. The FIBMOS device provides threshold stability, greater output resistance, and is more resistant against punchthrough effects and hot electron degradation. The FIBMOS device acts more like an ideal transistor than the conventional MOSFET.

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