GIZMo for DUNE at LBNF

Divas Subedi
Trinity College
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Supervisors
Michael J. Utes
Paul M. Rubinov

Table of Contents

1. Background

1.1 DUNE

The Deep Underground Neutrino Experiment (DUNE) is a leading-edge, international experiment for neutrino science and proton decay studies, which seeks to research several fundamental questions about the nature of matter and the evolution of the universe. DUNE will consist of two neutrino detectors placed in the world's most intense neutrino beam. One detector will record particle interactions near the source of the beam, at the Fermi National Accelerator Laboratory in Batavia, Illinois. A second, much larger, detector will be installed more than a kilometer underground at the Sanford Underground Research Laboratory in Lead, South Dakota [1]

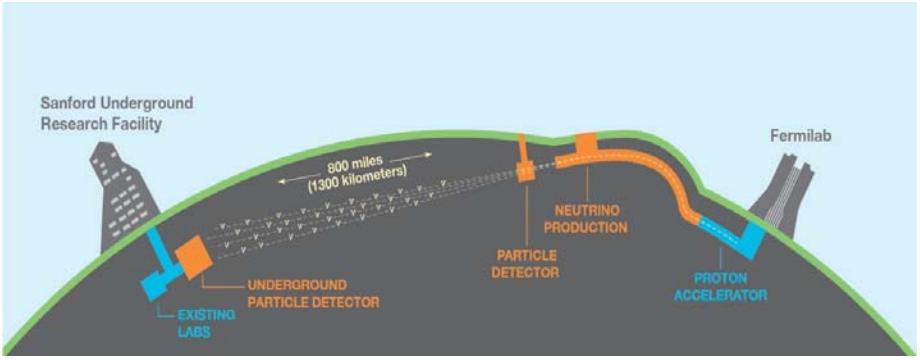

Figure 1 Deep Underground Neutrino Experiment

1.1 LArTPC

DUNE farside detector uses a Liquid Argon Time Projection Chamber to perform a three-dimensional reconstruction of neutrino trajectory or interaction using a combination of electric fields and magnetic fields. When a neutrino interacts with an argon atom, it creates a high-energy charged lepton. This charged lepton ionizes other argon atoms as it passes through the liquid, leaving a trail of free electrons and argon ions in its wake. The electrons are drawn into the wires by the strong electric field and register as a pulse of current in a particular wire.[2]

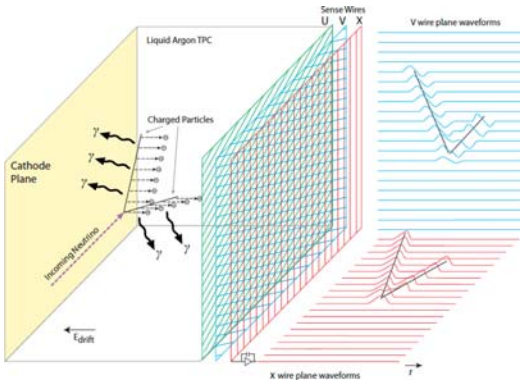

Figure 2 Liquid Argon Time Projection Chamber

2. Motivation

2.1 Ground Loop

Ground Loop occurs when two points of a circuit are intended to have the same reference potential but have a potential difference between them. Ground Loop is one of the major causes of noise in any signal system. Figure 3 shows a simple example of ground loop. The measurement of the signal (V_{sig}) is not isolated from the external circuit, as $V_{meas} = V_{sig} - V_G$ and V_G is dependent on current from the external circuit. The signal produced by DUNE's far-side detector is susceptible to this noise. To ensure adequate sensitivity of the detectors, ground systems must be put in place that will isolate the detectors from all other electrical systems and equipment, and minimize the influence of inductive and capacitive coupling and ground loops

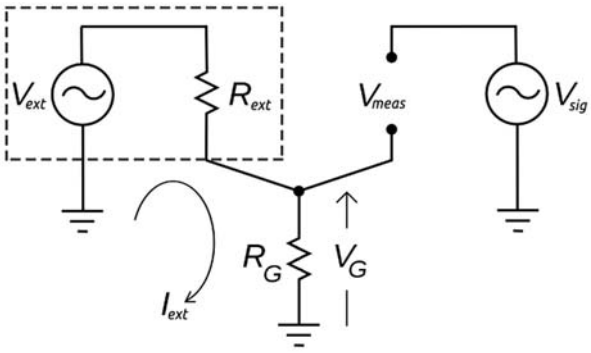

Figure 3 Example of Ground Loop

2.2 Single Point Grounding

One solution to ground loop is single-point-grounding. As the name suggests, all of the components of detectors are referenced at a single node. This reference node or the **Detector Ground** is isolated from the safety ground or the **Building Ground**. The Detector Ground consists of a steel containment vessel enclosing a cryostat, the cryostat, and all metal structures attached to or supported by the detector vessel. [3]

However, this isolation of Detector Ground raises a safety issue. In case of any fault, accumulation of charge might cause the potential of reference node to rise above the safety level, which poses a shock hazard. To resolve this, a safety mechanism is established using saturable inductors. The DUNE far side detector is connected to building ground for safety purposes using 2AWG wire in series with saturable inductors. This is the only desired connection to building ground. Any additional ground connections could create current loops and be a source of noise. The saturable inductor is designed to reduce noise by presenting some impedance to low level AC currents, but presenting only a minimal impedance to high amperage fault currents so that the main power circuit breaker will trip. [4]

3. Objective

The objective of Ground Impedance Monitor is to monitor the integrity of the single-point-grounding configuration required for low noise operations of the DUNE far side detector. GIZMo should monitor the impedance between the Detector Ground and the Building Ground in real-time to maintain the integrity of the signal.

4. Design

4.1 Circuit

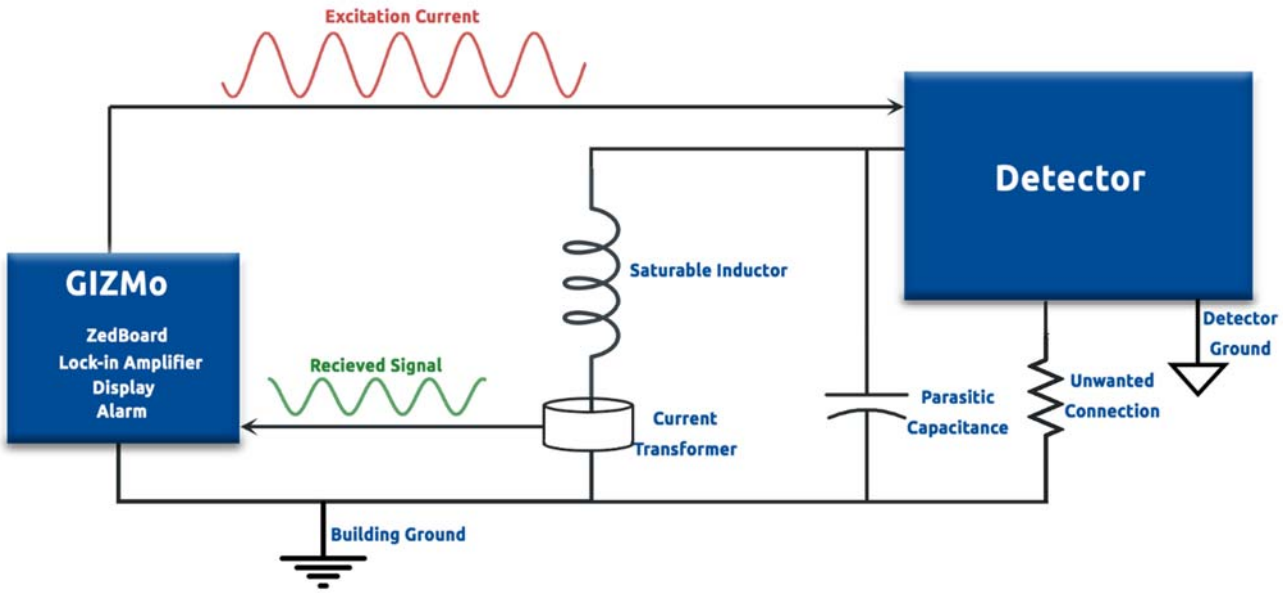

Figure 4 Simplistic circuit for operation of GIZMo

The primary constituent of GIZMo is listed as follow:

1. **ZedBoard**
   ZedBoard features the Zynq chip, a “System-on-Chip” that combines an FPGA and a dual-core ARM processor (XC7Z020). This is combined with a small number of **'PMOD'** modules to provide a low cost but powerful digital signal processing system. A 16bit DAC and a 12bit ADC operating at approximately 1MSPS forms the main interface to the circuit
2. **Lock-in Amplifier**
   Lock-in amplifier is a type of amplifier that can extract a signal with a known carrier wave from an extremely noisy environment. Given the information on waveform and frequency of incoming signal is known, it makes for an exceptional filtering device.
3. **Current Transformer**
   A current Transformer is used to measure the current flowing through the saturable inductor while providing minimum disturbance to the circuit itself.

4.2 Operation Mechanism

The excitation waveform is stored in one FPGA block RAM. It is injected into the circuit through the DAC. The incoming signal is digitized using the ADC and is stored in another Block RAM. The DAC and ADC are controlled by FPGA firmware to guarantee precise timing for the generation and digitization of the relevant waveforms. The results of acquisition are transferred to the Linux system running on the ARM processer portion of the Zynq chip. The digitized waveform is demodulated in software and a low pass filter is applied to derive an I and Q measurement. The quadrature of I and Q is used as a measurement of the wave amplitude. The magnitude and the phase difference between the signal and the excitation waveform are used to estimate the impedance. [4]

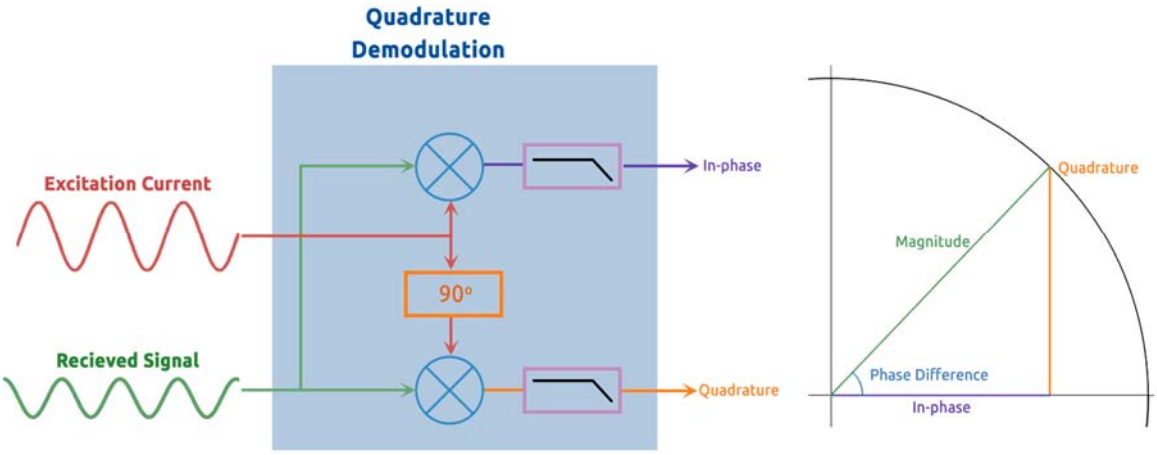

Figure 5 Quadrature demodulation of the signal

4.3 Additional Feature

Additional Feature for GIZMo involves:

- **Display**
  An LED display to show the estimated value of the impedance. This will be used for debugging as well as monitoring purposes.
- **Speaker**
  It is important to understand that an unwanted ground connection exists as soon as it occurs. So, the speaker can be used to alert user about the unwanted connections.
- **Alert Beacon**
  Alert Beacon serves the same purpose as the speaker but provides visible indication instead of auditory.

5. Internship Project Specification

Objectives for my internship were to:

- Implement the signal processing model for impedance estimation
- Implement a real-time monitoring system via use of ZedBoard

6. Development

6.1 Program Design

During the first half of the internship, I worked on implementing the code for impedance detection using Python, SciPy, and LTSPICE. The later weeks were spent on implementing the system on a MiniZed, an SoC with a similar architecture to that of ZedBoard.

6.1.1 Modeling the circuit in LTSPICE

The Howland Current Pump was used to simulate the excitation waveform from GIZMo. The rest of the circuit was built similar to figure 4. Figure 6 shows the LTSPICE circuit. Here, **`Lsat`** models saturable inductor, **`Cdet`** models the detector, and **`Rshort`** and **`Cshort`** model the resistive and capacitive component of the unwanted impedance respectively.

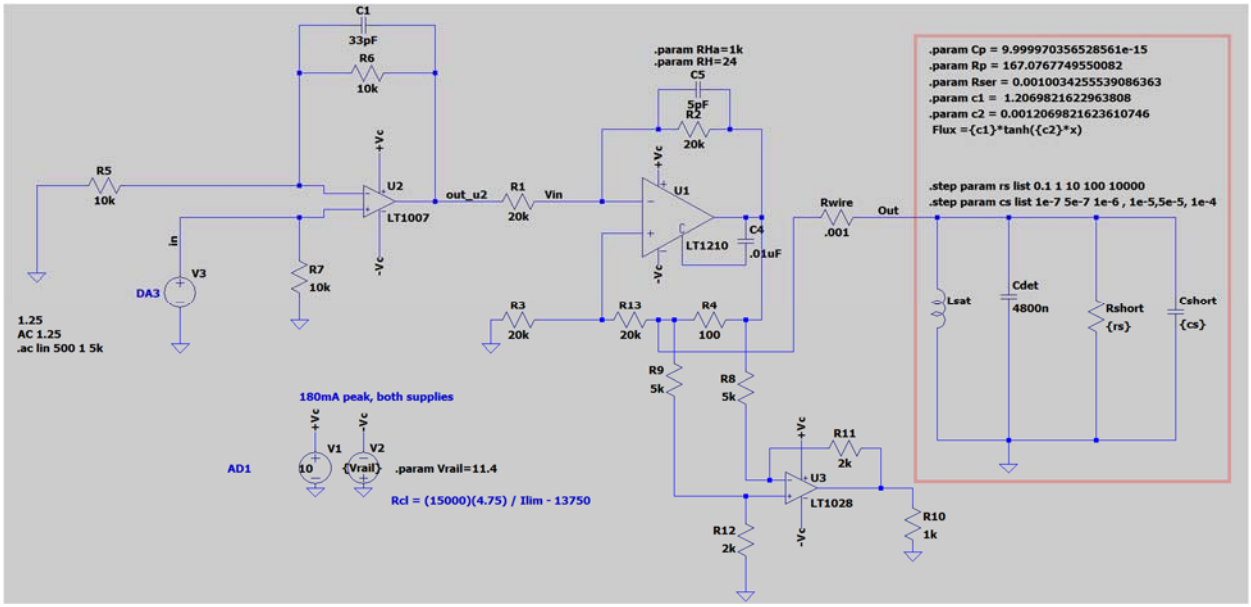

Figure 6 LTSPICE model for connection between GIZMo and Detector

Frequency sweep was performed with varying values for unwanted impedance to find the operating frequency for the excitation waveform. With the current estimation of the parasitic capacitance of DUNE (≈ 4800 nF), the best operating frequency was determined to be around 3000 Hz. As shown in

figure 7, this frequency is out of the region where the reactive load of unwanted impedance and parasitic capacitance of the detector resonate with the saturable inductor (0.5kHz to 2.7 kHz).

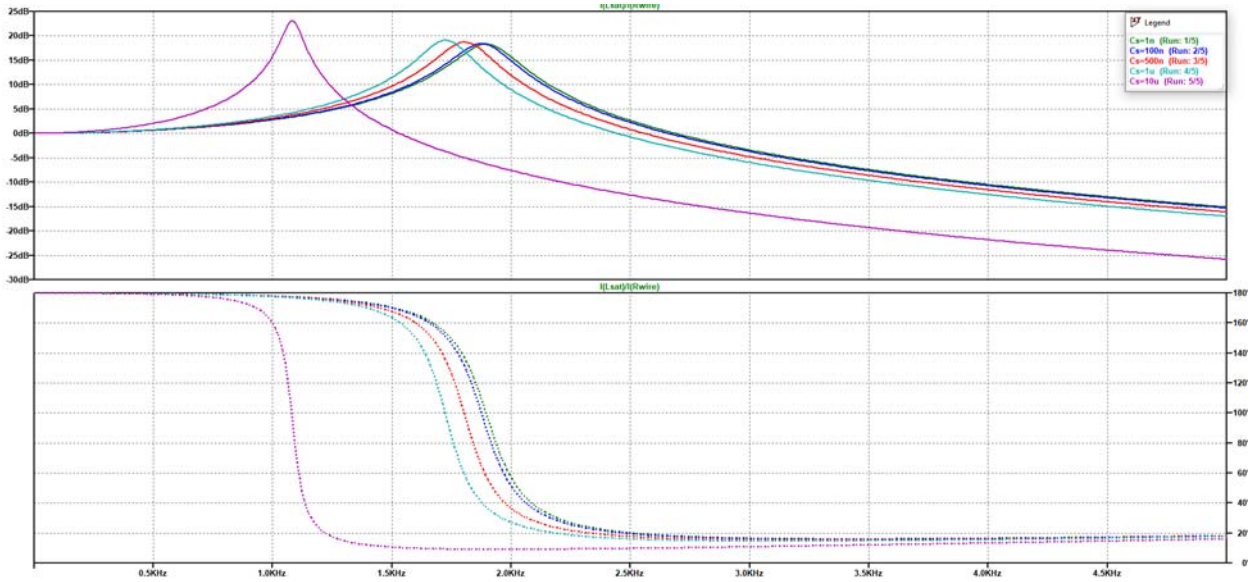

Figure 7 Magnitude ratio and phase difference for varying capacitive load

6.1.2 Impedance Estimation

Python along with SciPy was used for signal processing. The transient response of the LTSPICE simulation is used to estimate the impedance. Filter from SciPy was used to simulate the behavior of the lock-in amplifier. Quadrature demodulation is performed and calibration curves are generated using Python as shown in figure 8 and 9.

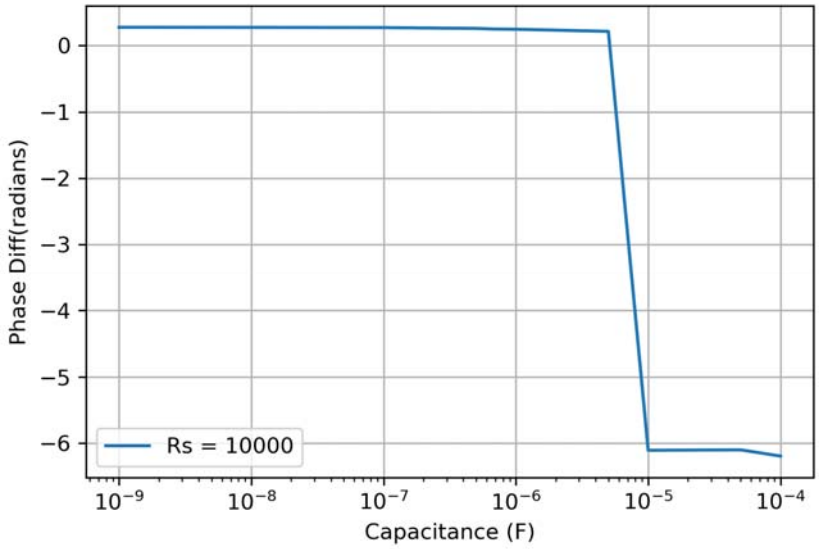

Figure 8 Calibration curve for capacitive component

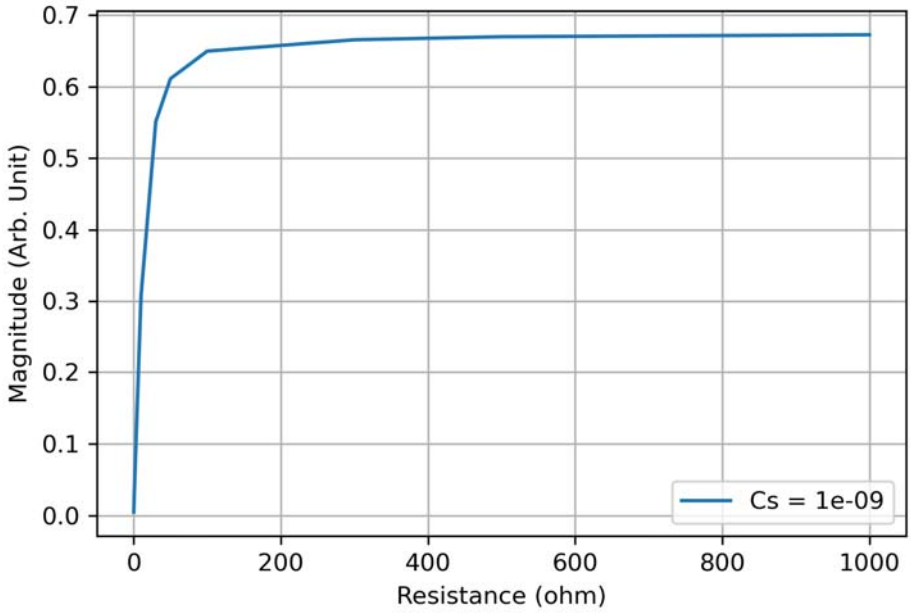

Figure 9 Calibration Curve for resistive component

6.1.2 Developing the images for MiniZed

Requirements for the boot image:

1. Able to run Python3 for DSP
2. Run the GIZMo scripts at startup
3. Able to interface with PMOD

The hardware description is defined using Vivado. The hardware description includes the code for interfacing with PMODs, and Block memory. Petalinux uses the hardware description provided by Vivado to create a boot image and Linux kernel. Petalinux tools allows installation of Python3 on Linux Kernel made for Zynq SoC.

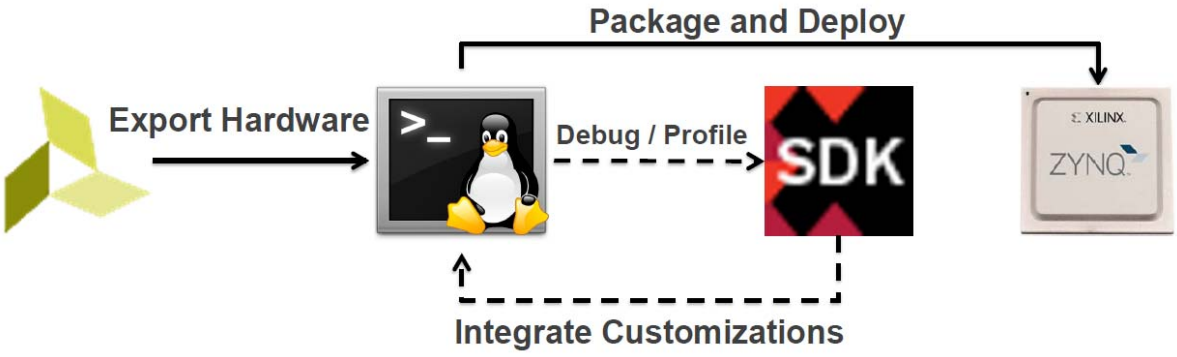

Figure 10 Linux Application Development Workflow

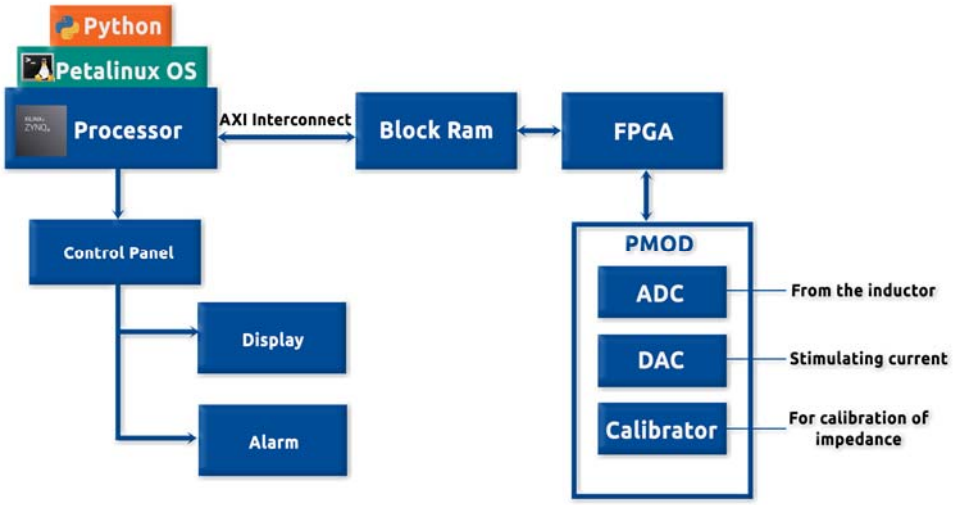

Figure 11 Data flow on ZedBoard

6.2 Development Challenges

One of the hardest problems to tackle was to model the saturable inductor in LTSPICE due to its nonlinear nature. A Python program was designed to address this problem.

6.3.1 Circuit Element Parameter Optimization

The Python program bridges LTSPICE and Python. Once the circuit with parameterized element is built in LTSPICE, Python can be used to estimate the parameter for the circuit element so that it would emulate the behavior of the real circuit element. The algorithm for this optimization is shown in figure 15. The algorithm uses the Newton Conjugate-Gradient method to get a new set of parameters from old ones.

$$f(\mathbf{x}) \approx f(\mathbf{x}_0) + \nabla f(\mathbf{x}_0) \cdot (\mathbf{x} - \mathbf{x}_0) + \frac{1}{2}(\mathbf{x} - \mathbf{x}_0)^T \mathbf{H}(\mathbf{x}_0)(\mathbf{x} - \mathbf{x}_0).$$

Equation 1 Newton Conjugate-Gradient Method

For this project, we needed to parameterize the inductor component (**`Lsat`**) to emulate the behavior of the saturable inductor. The LTSPICE model of the inductor component has properties as shown in figure 12. The inductance is modeled using its magnetic flux as a function of current. A simple circuit involving the saturable inductor is used to get the required data for optimization. Figure 13 shows the physical implementation and LTSPICE model of the simple circuit. The parameters **`Cp`**, **`Rp`**, **`Rser`**, **`c1,`** and **`c2`** as shown in figure 13 are estimated. The objective function, in this case, is taken as the sum of normalized least squared difference in magnitude ratio and phase difference between voltage reading at P1 and P2. Figure 14 shows the magnitude ratio and the phase difference across frequency after optimization.

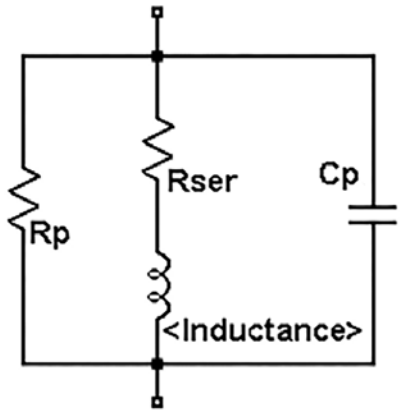

Figure 12 LTSPICE inductor component model

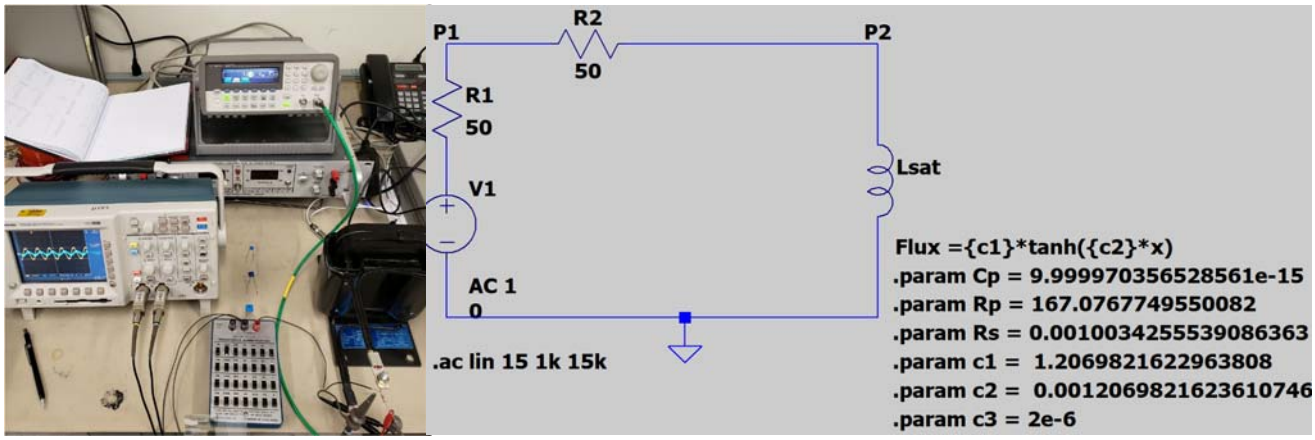

Figure 14 Physical(left) and LTSPICE Model(right) circuit for estimation of parameters of Saturable current

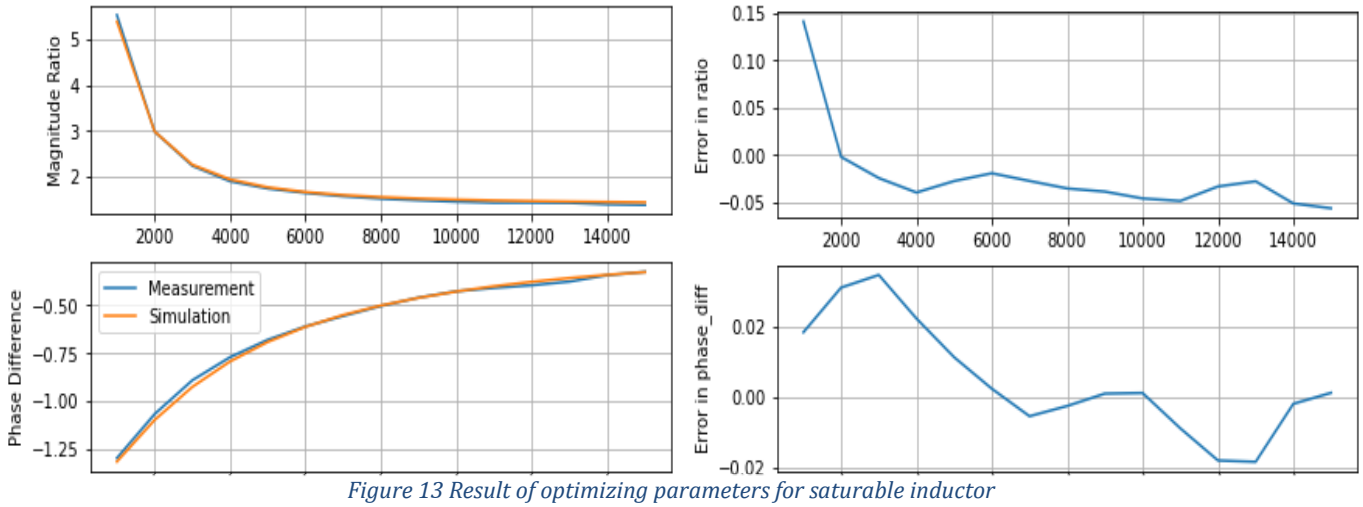

Figure 13 Result of optimizing parameters for saturable inductor

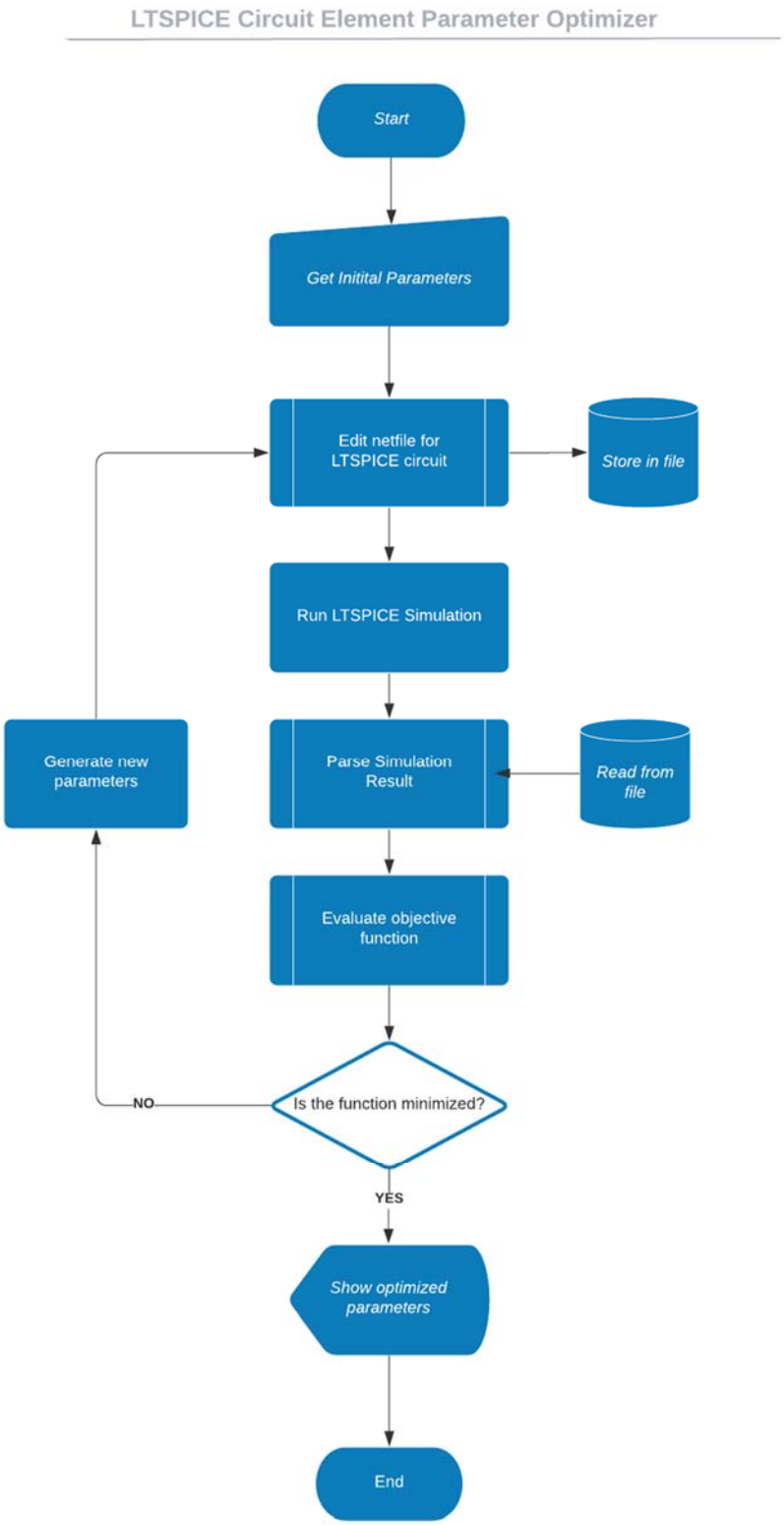

Figure 15 Flowchart for optimization of circuit element parameters

7. Technologies Used

Name	Purpose
Python	Digital Signal Processing
Vivado	Hardware Description Designing
Vitis	Design software for FPGA
Petalinux	Package and deploy boot image
Git	Version Control

8. Future Works

Ideally, we would like to fully deploy the built images on ZedBoard. Once, that is done, fidelity of signal processing script can be tested. The system, then, would be ready for calibration.

Additionally, we hope to package the Python program to optimize the circuit element and publish a technical memo on it.

9. Conclusion

In order to maintain noiseless environment for DUNE far side detector, a detector ground, isolated from the building ground, is established. GIZMo is to be deployed to monitor the integrity of the detector ground. Python script is implemented for impedance estimation. Boot image and Linux kernel is built using Vivado and Petalinux for ZedBoard, on which Python scripts will run.

10.Acknowledgment

I would like to thank my supervisors – Michael J. Utes, and Paul M. Rubinov for being great advisors and mentors. Their guidance and advice carried me through all stages of my project. I am grateful to them for not only helping me in my project but also helping me to explore academic career path.

Special thank you to my internship mentors Michal Geelhoed, Ahmed Syed, and Linden Carmichael for all the guidance throughout this summer.

Additionally, I would like to thank all members of the SIST committee whose dedication and effort made this internship program possible.

11. References

[1] Deep Underground Neutrino Experiment (DUNE) Homepage: https://www.dunescience.org/

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[3] T. Shaw, Grounding 35T, DUNE & ProtoDUNE : https://indico.cern.ch/event/459004/contributions/1972384/attachments/1183329/1715700/tms-dune-grounding_v1.pdf

[4] P. Rubinov, M. Utes, Ground Impedance Monitor ICEBERG Edition